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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/256,265	02/23/99	KAO D	15917-11

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EXAMINER	
DIAZ,J	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 10/03/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/256,265	Applicant(s) KAO ET AL.	
	Examiner José R. Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *09 June 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *3-7 and 11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Election/Restrictions

➢ Applicant's election with traverse of June 15, 1999 in Paper No. 3 is acknowledged. The traversal is on the ground(s) that a search for the subject matter of any of the alleged groups would require the same field of search as the other groups. This is not found persuasive because the MPEP established that showing diverse classification is sufficient to establish a burden on the Examiner (MPEP 808.02).

The requirement is still deemed proper and is therefore made FINAL.

Drawings

➢ The drawings are objected to by the Draftsperson under 37 CFR 1.84. Applicant is required to submit a proposed drawing correction in reply to this Office Action.

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➢ Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Middelhoek et al. (US Patent No. 5,216,269).

Regarding claim 1, Middelhoek et al. teach a substrate; a defined channel region; a floating gate (11) disposed over said channel region separated therefrom by a first insulating layer (21); a control gate (12) placed on one side of said floating gate (11) separated therefrom by a second insulating layer (22); a erase gate (14) placed on second side of said floating gate (11) separated therefrom by said second insulating layer (22); a drain region (6) disposed on a first side of said floating gate (11); and a source region (5) disposed on a second side of said floating gate (11) (Figure 10).

➢ Claims 8 and 10 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chang (US Patent No. 6,125,060).

Regarding claim 8, Chang teaches a memory array (214) comprising a plurality of memory cells each having a floating gate (103), an erase gate (122), a control gate (101), a source region (105), and a drain region (108) (Figure 1f) comprising: a plurality of rows and columns of interconnected memory cells wherein the control gates (CG(i)) of memory cells in the same row are connected by a common word-line (201); the erase gates (EG(m)) of memory cells in the same row are connected by a common erase-line (207); the source regions (Source(m)) of memory cells in the same row are connected by a common source-line (205); the drain regions (208) of memory cells in the same row are connected by a common drain-line (BL (i)); and control circuit connecting to

circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array (Figure 3).

Regarding claim 10, Chang teaches that said erase gate (122) overlaps said floating gate (103) and said control gate (101) (Figure 1f).

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

➢ This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Middelhoek et al. (US Patent No. 5,216,269) in view of Chang (US Patent No. 6,125,060).

Middelhoek et al., as stated supra, essentially discloses the claimed invention but fails to show a transistor wherein an erase gate overlaps a floating gate and a control gate. Regarding claim 10, Chang teaches that said erase gate (122) overlaps said floating gate (103) and said control gate (101) (Figure 1f).

Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Middelhoek et al. to include a transistor wherein a erase gate overlaps a floating gate and a control gate, as taught by Chang, since such modification would result in a memory device having low currents for both program and erase operations, as described in column 2, lines 5-10 of Chang.

- Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US Patent No. 6,125,060) in view of Middelhoek et al. (US Patent No. 5,216,269).

Chang, as stated supra, essentially discloses the claimed invention but fails to show an erase gate placed on a second side of a floating gate separated therefrom by a second insulation layer. Regarding claim 9, Middelhoek et al. teach a substrate; a defined channel region; a floating gate (11) disposed over said channel region separated therefrom by a first insulating layer (21); a control gate (12) placed on one side of said floating gate (11) separated therefrom by a second insulating layer (22); a erase gate (14) placed on second side of said floating gate (11) separated therefrom by said second insulating layer (22); a drain region (6) disposed on a first side of said floating gate (11); and a source region (5) disposed on a second side of said floating gate (11) (Figure 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Chang to include an erase gate placed on a second side of a floating gate separated therefrom by a second insulation layer, as taught by Middelhoek et al., since such modification would result in a memory device wherein a feed-back loop is formed using hot-carrier injection to prevent over-erasure, as described in column 4, lines 35-44 of Middelhoek et al.

Conclusion

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Otani et al. (US Patent No. 5,708,285) disclose a non-volatile semiconductor information storage device. Yoshikawa (US Patent No. 5,229,632) discloses an electrically erasable memory device having erasable-electrode connected to substrate junction. Amin et al. (US Patent No. 5,455,793) disclose an electrically reprogrammable EPROM cell with merged transistor and optimum area. Simko (US Patent No. 4,099,196) discloses a triple layer polysilicon cell. Samachisa et al. (US Patent No. 5,579,259) disclose a low voltage erase of a flash EEPROM system having a common erase electrode for two individually erasable sectors. Yim et al. (US Patent No. 5,109,361) disclose an electrically page erasable and programmable read only memory. Arima et al. (US Patent No. 5,252,847) disclose an electrical erasable and programmable read only memory. Park (US Patent No. 5,874,759) discloses a flash memory cell. Momodomi et al. (US Patent No. Re. 35,838) disclose an electrically erasable programmable read only memory with NAND cell structure.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mahshid Saadat can be reached on (703) 308-4915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
September 27, 2000

Mahshid Saadat

Mahshid Saadat
Supervisory Patent Examiner
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